REMARKS

Claims 1-10 and 17-26 are pending. Claims 1, 4, 5, 7, 18, 19, and 21 are amended. Claims 22-26 are new. Claims 11-16 are canceled. Applicant reserves the right to pursue original and other claims in this and other applications.

Claims 1-4 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6369409 ("Takasu '409") in view of U.S. Published Patent App. No. 2002/0000671 ("Zuniga '671"). This rejection is respectfully traversed.

Claim 1 recites a semiconductor apparatus, comprising:

> a semiconductor substrate;
>
> a metal wiring layer formed over the semiconductor substrate;
>
> a material layer formed over the metal wiring layer and having a window therein;
>
> a first electrode pad formed over the semiconductor substrate, and exposed through said window for providing contact between said semiconductor apparatus and external circuitry; and
>
> a circuit formed over said semiconductor substrate and in a region under the window in the material layer exposing the first electrode pad, said circuit comprising an array of adjacent resistive elements formed of a semiconductor material, said first electrode pad being formed over said array of resistive elements such that said first electrode pad extends transversely across said array.

Applicant submits that Takasu '409 and Zuniga '671, even in combination, fail to teach or suggest "a first electrode pad formed over the semiconductor substrate, and exposed through said window for providing contact between said semiconductor apparatus and external circuitry," and "a circuit formed over said semiconductor substrate and in a region under the window in the material layer exposing the first electrode pad, said circuit comprising an array of adjacent resistive elements formed of a semiconductor material," as recited in claim 1. As Applicant teaches in the Specification of this application, the location of the circuit under the first electrode pad provides for prevention of "contamination by ion impurities, charges, moisture, and hydrogen to the resistors 9 from a side above the electrode pad 31," (Specification, at ¶ 0078) and allows a semiconductor

apparatus to be manufactured "smaller in area than the conventional semiconductor device..." (Specification, at ¶ 0084).

The Office asserts that the aluminum layer 814 (shown in Figure 12F of Takasu '409) and the polysilicon resistors 807 (shown in Figure 12D of Takasu '409) teach, respectively, the "first electrode pad" and the "circuit formed over said semiconductor substrate and in a region under the window in the material layer exposing the first electrode pad" recited in claim 1. Office Action of September 30, 2008, at 2-3. Figures 12D and 12F of Takasu '409 are reproduced below.

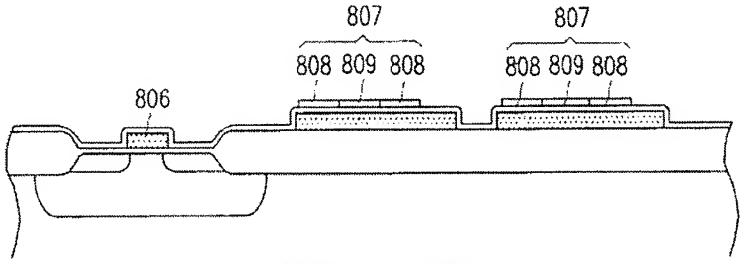


FIG. 12D

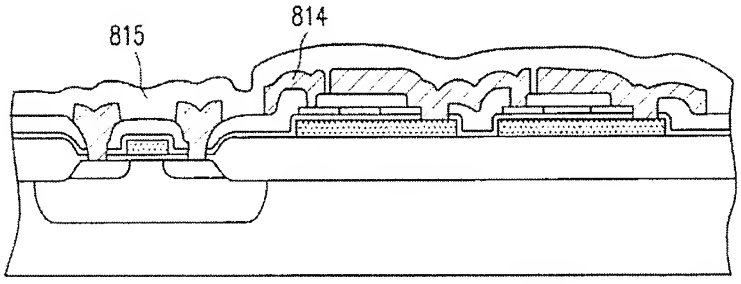


FIG. 12F

Applicant submits that the aluminum layer 814 is not "a first electrode pad," as recited in claim 1. Rather, the aluminum layer 814 is, at most, a metal wiring layer. The Office acknowledges as much. *See*, Office Action of September 30, 2008, at 3 ("it is implicit that the aluminum 'wiring' provides contact between an integrated circuit and external circuitry").

Furthermore, Applicant submits that the aluminum layer 814 is not "a first electrode pad formed over the semiconductor substrate, and exposed through said window for providing contact between said semiconductor apparatus and external circuitry," as recited in claim 1. To the contrary, Takasu '409 shows the region of the aluminum layer 814 overlying the polysilicon resistors 807 as entirely covered by protective film 815. *See*, Takasu '409, Fig. 12F (above). While Takasu '409 suggests that "although it is not illustrated, the protective film 815 of a region such as a bonding pad is removed," (Takasu '409, Col. 9, lines 54-56), Takasu '409 fails to teach or suggest the location of the "bonding pad." Applicant submits that nothing in Takasu '409 teaches exposing any of the portions of the aluminum layer 814 "through a window" of protective film 815 or using the exposed portion to provide "contact between said semiconductor apparatus and external circuitry," as recited in claim 1.

Furthermore, Applicant submits that the most likely location of the "bonding pad" of Takasu '409, and the most logical region of the semiconductor device for "providing contact between said semiconductor apparatus and external circuitry," is gate electrode 806. As shown in Figure 12D of Takasu '409 (above), the element of Takasu '409 alleged to correspond to the "circuit" of claim 1 (i.e., polysilicon resistors 807) are not formed in a region under gate electrode 106.

Thus, Takasu '409 fails to teach or suggest "a first electrode pad formed over the semiconductor substrate, and exposed through said window for providing contact between said semiconductor apparatus and external circuitry," or "a circuit formed over said semiconductor substrate and in a region under the window in the material layer exposing the first electrode pad," as recited in claim 1. Zuniga '671 fails to remedy the deficiency of Takasu '409, and is not cited as such.

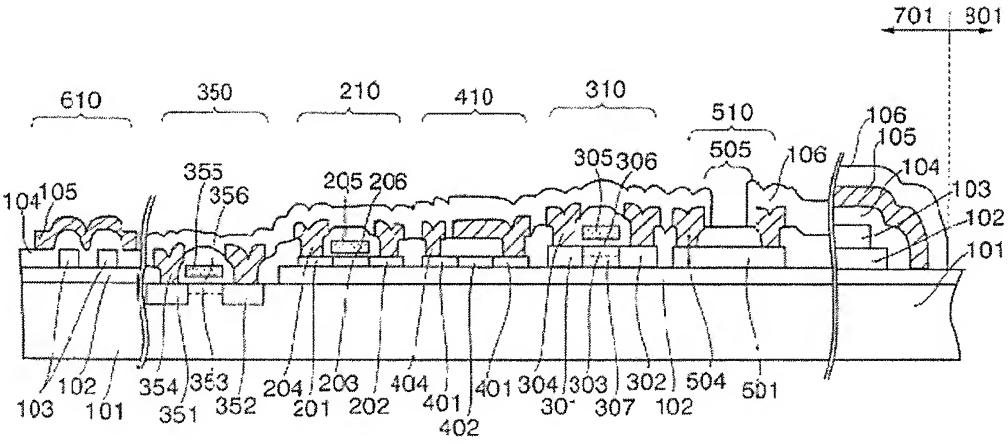
Therefore, Applicant submits that claim 1 is allowable over the cited combination. Claims 2-4 and 17 depend from claim 1, and are allowable over the cited combination for at least the reasons discussed above. Accordingly, Applicant respectfully requests that the § 103(a)

rejection of claims 1-4 and 17 as being unpatentable over Takasu '409 in view of Zuniga '671 be withdrawn.

Claims 1-6, 17, 19, and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Published Patent App. No. 2002/0145177 ("Takasu '177") in view of Zuniga. This rejection is respectfully traversed.

The elements of claim 1 are discussed above. Claim 19 recites a semiconductor apparatus, comprising, *inter alia*, "an insulating layer ... having an electrode-pad formation region, wherein the electrode-pad formation region is formed over the resistive-element formation region, and wherein the electrode-pad formation region has an electrode pad comprising a metal layer providing contact between said semiconductor apparatus and external circuitry ... and a passivation film formed over an uppermost metal wiring layer of the semiconductor apparatus and having a window arranged to expose the electrode pad."

Takasu '177, like Takasu '409, fails to teach or suggest "a circuit formed over said semiconductor substrate and in a region under the window in the material layer exposing the first electrode pad," as recited in claim 1, or an "an electrode pad comprising a metal layer providing contact between said semiconductor apparatus and external circuitry" as recited in claim 19. The Office asserts that this element is shown in Figure 1 of Takasu '177. Specifically, the Office asserts that the "aluminum film 105 connected to regions 401 and arranged to cover region 402" corresponds to the "first electrode pad" of claim 1 (Office Action of September 30, 2008, at 4, 7); the Office also asserts that the "bleeder resistance circuit" described in ¶ 0063 of Takasu '177 describes a "circuit formed over said semiconductor substrate and in a region under the electrode pad," (*id.* at 5, 7). Figure 1 of Takasu '177 is reproduced below.



The asserted "bleeder resistance circuit" is formed in the area indicated by reference numerals 401 and 402 in the figure shown above. Takasu '177, at ¶ 0061 ("In the single crystal silicon device forming layer 103 formed on the silicon substrate 101 through the buried oxide film 102, a pair of high concentration impurity regions 401 and a low concentration impurity region 402 sandwiched therebetween are formed, thereby forming a resistor. Although only one resistor is shown for simplicity here, a bleeder resistance is formed by a plurality of resistors in actuality."). This alleged circuit is not formed "over the semiconductor substrate, and exposed through said window for providing contact between said semiconductor apparatus and external circuitry," as recited in claim 1, or under the "electrode pad comprising a metal layer providing contact between said semiconductor apparatus and external circuitry" as recited in claim 19. Zuniga fails to remedy the deficiency of Takasu '177, and is not cited as such.

Therefore, Applicant submits that claim 1 is allowable over the cited combination. Claims 2-6 and 17 depend from claim 1, and claim 20 depends from claim 19. These dependent claims are allowable over the cited combination for at least the reasons discussed above with regard to their respective independent claims. Accordingly, Applicant respectfully requests that the § 103(a) rejection of claims 1-6, 17, 19, and 20 as being unpatentable over Takasu '177 in view of Zuniga '671 be withdrawn, and the claims allowed.

Claim 7 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Takasu '177 in view of Zuniga '671, further in view of U.S. Published Patent App. No. 2002/0063262 ("Matsuzaki"). This rejection is respectfully traversed.

Claim 7 depends from claim 1, and is allowable over the combination of Takasu '177 and Zuniga '671 for at least the reasons discussed above with regard to claim 1. Matsuzaki fails to remedy the deficiencies of the asserted combination, and is not cited as such. Accordingly, Applicant respectfully requests that the § 103(a) rejection of claim 7 be withdrawn, and the claim allowed.

Claims 8-10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Takasu '177 in view of Zuniga '671, further in view of U.S. Patent No. 6,232,823 ("Tsuchida"). This rejection is respectfully traversed.

Claims 8-10 depend from claim 1, and are allowable over the combination of Takasu '177 and Zuniga '671 for at least the reasons discussed above with regard to claim 1. Tsuchida fails to remedy the deficiencies of the asserted combination, and is not cited as such. Accordingly, Applicant respectfully requests that the § 103(a) rejection of claims 8-10 be withdrawn, and the claims allowed.

Claims 18 and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Takasu '177 in view of Zuniga '671, further in view of U.S. Patent No. 5,107,313 ("Kohda"). This rejection is respectfully traversed.

Claims 18 and 21 depend from claims 1 and 19, respectively, and are allowable over the combination of Takasu '177 and Zuniga '671 for at least the reasons discussed above with regard to their respective independent claims. Kohda fails to remedy the deficiencies of the asserted combination, and is not cited as such. Accordingly, Applicant respectfully requests that the § 103(a) rejection of claims 18 and 21 be withdrawn, and the claims allowed.

Applicant notes that new claims 22-26 depend from claim 1, and are allowable over the cited references for at least the reasons discussed above with regard to claim 1, as well as on their own merits. For example, claim 22 recites the semiconductor apparatus of claim 1, "wherein the first electrode pad is formed on an uppermost metal wiring layer of the semiconductor apparatus, and wherein said uppermost metal wiring layer is substantially entirely covered by said material layer." The cited combination of references fails to teach or suggest an uppermost metal wiring layer substantially entirely covered by a material layer, and a first electrode pad exposed in a window of the material layer and above a circuit. Rather, at most, the cited combinations teach that the circuit is underneath the uppermost metal wiring, not the first electrode pad. Accordingly, allowance of claims 22-26 is respectfully requested.

In view of the above amendment, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

By _____

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